*Arab Academy for Science Technology and Maritime Transport (AASTMT)*

*College of Computing and Information Technology (CCIT)*

***Operating Systems CS322***

***Sheet 1***

***Question 1: Answer the Following Questions:***

* 1. List and briefly define the four main elements of a computer.
  2. What is an interrupt?
  3. How are multiple interrupts dealt with?
  4. What characteristics distinguish the various elements of a memory hierarchy?
  5. What is cache memory?

***Question 2: Solve the Following Problems:***

* 1. Suppose the hypothetical processor of figure 1.3 also has two I/O instructions and a subtract instruction:

0011 = Load AC from I/O.  
0111 = Store AC to I/O.  
0100 = Subtract contents of addressed word from AC.

In this case the 12-bit address identifies a particular external device. Show the program execution for the following program:

1. Load AC from device 4.
2. Subtract contents of memory location 960.
3. Store AC to device 5.

Assume that the next value retrieved from device 5 is 10 and at location 960 contains the value of 1.

* 1. In virtually all systems that includes DMA modules, DMA access to main memory is given higher priority that processor access to main memory. Why?
  2. A DMA module is transferring characters to main memory from an external device transmitting at 9600 bits per second (bps). The processor can fetch instructions at the rate of 1 million instructions per second. By how much will the processor be slowed down due to the DMA activity?
  3. A computer consists of a CPU and an I/O device *D* connected to main memory *M* via a shared bus with a data bus width of one word. The CPU can execute a maximum of 106 instructions per second. An average instruction requires five processor cycles, three of which use the memory bus. A memory read or writes operation uses one processor cycle. Suppose that the CPU is continuously executing “background” programs that require 95% of its instruction execution rate but not any I/O instructions.

Assume that one processor cycle equals one bus cycle. Now suppose that very large blocks of data are to be transferred between *M* and *D*.

**a.** If programmed I/O is used and each one-word I/O transfer requires the CPU to execute two instructions, estimate the maximum I/O data transfer rate, in words per second, possible through

**b.** Estimate the same rate if DMA transfer is used.

**1.5** Consider a memory system with the following parameters:

*Tc* \_ 100 ns *Cc* \_ 0.01 cents/bit

*Tm* \_ 1200 ns *Cm* \_ 0.001 cents/bit

**a.** What is the cost of 1 MByte of main memory?

**b.** What is the cost of 1 MByte of main memory using cache memory technology?

**c.** If the effective access time is 10% greater than the cache access time, what is the hit ratio *H*?

**1.6** A computer has a cache, main memory, and a disk used for virtual memory. If a referenced word is in the cache, 20 ns are required to access it. If it is in main memory but not in the cache, 60 ns are needed to load it into the cache (this includes the time to originally check the cache), and then the reference is started again. If the word is not in main memory, 12 ms are required to fetch the word from disk, followed by 60 ns to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9 and the main-memory hit ratio is 0.6.What is the average time in ns required to access a referenced word on this system?